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ELECTROTHERMAL AND PHASE TRANSITION NUMERICAL MODEL FOR MEMRISTOR APPLICATION

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Today memristor is widely considered as the most important component in brain-like artificial networks because of its similarity to biological synapse. For this reason, several memristor prototypes such as resistive memristor, polymeric memristor, ferroelectric memristor, and spintronic memristor have been theoretically proposed, subsequently followed by their respective physical realization. Most recently, memristor device using phase-change media has received more interest compared to its seniors due to its fast switching speed, low energy consumption, and long retention time. However, a comprehensively physics-based model that can explain the memristive behaviour of the phase-change memristor remains missing. In order to address this issue, we have proposed a computational pseudo-3D model to simulate the physical performances of the phase-change memristor that involves the electrical, thermal, and phase transition processes. According to this developed model, the ability for phase-change memristor to exhibit a pinched I-V hysteresis loop as well as several advantages over other memristors have been demonstrated.

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1. Introduction

The vigorous developments on computer industry have been witnessed over the past twenty years in terms of the storage capacity, the processing speed, the power consumption, and the cost [1]. Owing to these exciting advances, the dream to make use of computer to replace human brain, i.e., building computers that learn, reason, and even emote to solve problems in the way human does, may come true in the near future. However, the challenge for building artificial brain arises from the difficulty in integrating more electronic components in a single chip. The amount of the CMOS transistors that can be integrated in a single chip is determined by the well known Moore's law that the capacity of a storage device doubles every two years [2]. However, as the size of the CMOS transistor can not be reduced below a given technology node due to the scaling limits [3, 4], the current consensus is that Moore's law will soon lose its efficacy. Consequently, the practicality of using CMOS-based architecture to emulate the human brain with ~ 10^{11} neurons and 10^{15} synapses remains as a question [5]. In this case, memristor, as the fourth fundamental circuit element besides resistor, capacitor, and inductor, has been extensively considered as an alternative solution to realizing the brain-inspired neuromorphic system. The concept of memristor can retrospect to 1970th when Chua predicted the existence of the memristor mathematically [6], while its physical instance has not been found until 2008 when HP researchers has for the first time fabricated a memristor-like device using resistive materials [7]. Inspired by this invitation, memristor has gained considerable interest from researchers worldwide and some other memristor prototypes besides resistive memristor have been developed [8-10], which can be classified as polymeric memristor, ferroelectric memristor, and spintronic memristor.

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The beauty of memristor stems from its superior scalability, low power consumption, and similar dynamic response to human brain. First, the scalability of memristor cell down to 10 nm or below has already been demonstrated [11], thus leading to an integration density several orders of magnitude higher than the current Flash technology. Moreover, the ability of memristor to maintain the previous state without the power supply allows for a lower power consumption compared to dynamic random access memory (DRAM) that requires charge to sustain its state. Most importantly, the fact that the memristance dynamically changes with the applied stimulus makes memristor a suitable replacement for the biological synapse whose state depends on how closely any two neurons are linked. For above reasons, memristor has been implemented for a wide range of applications including non-volatile memory, dynamic load, neuromorphic system, and image processing.

It should be noted that compared to other memristors, resistive memristor has attained more attention, as the electrical and thermal properties of the resistive materials have been deeply investigated over the past 20 years. In spite of these remarkable achievements, resistive memristor is inevitably facing several barriers. One drawback arises from its relatively low switching speed [12]. The volatility-to-switching speed ratio for memristor cells, in the HP cross-bar structure is around 10^3, which is much lower than the ratio for DRAM cells, i.e., 10^6. In addition, the endurance cycle of the resistive memristor is far behind DRAM (about 10^{10} cycles) [12]. Therefore, in order to improve the physical performance of conventional memristors, and thus to more closely mimic biological synapses, it is necessary to explore the alternative memristor devices so as to open a new route for building next generation electronic brain system. In this case, phase-change materials, which have already been extensively employed in optical discs [13, 14] and phase-change random access memory (PCRAM) [15, 16], might be an encouraging contender for memristor applications.

2. Simulation strategy

Today, phase-change materials have been extensively adopted in many types of mass storage devices such as optical discs, PCRAM, and scanning probe phase-change memory [17, 18]. The most appealing feature of phase-change materials arises from a fact that its resistance can be switched between a highly resistive state (i.e., amorphous state) and a highly conductive state (i.e., crystalline state) for an external electrical pulse. As a result, these two states can be used to denote binary bits (i.e., “0” and “1”) to realize the storage function. The resistance of phase-change materials can be changed continuously by varying the magnitude or the duration of the applied pulse, and can remember its last state even if encountering a power cut, leading to a very similar behaviour to the biological synapse. Among the families of phase-change materials, the $Ge_2Sb_2Te_5$ (also known as GST) alloy has been commonly regarded as the “gold standard” phase-change materials against which other alloys are often compared [19]. This is expected as compared to its counterparts, GST alloy usually exhibits a faster switching speed, longer data retention time, and higher reading contrast. For this reason, the GST alloy is considered as the active media used in our design.

The schematic of the designed memristor device using GST is illustrated in Figure 1. The key layout of this memristor consists of a GST layer sandwiched by a diamond-like carbon (DLC) capping layer and a DLC bottom layer. Both the top electrode and the bottom electrode are made of titanium tungsten (TiW), and all the layers are finally deposited on a silicon (Si) wafer. The thickness of the GST layer needs to be thin such that the required threshold voltage can be reduced, thus lowering the energy consumption. As a result, a 10 nm thick GST layer is implemented here, which is also a typical thickness for PCRAM [16]. The DLC capping layer is mainly devised to prevent diffusion and electromigration of materials into the GST region. In addition, because of its relatively low thermal conductivity [20], the DLC capping layer can effectively reduce the heat dissipation from GST layer to TiW electrode, and therefore induce a

high temperature inside the GST region. The DLC bottom layer acts primarily as a series resistor in order to limit the writing current. In this case, the thicknesses of the capping and bottom layers are considered to be 5 nm and 10 nm, respectively.

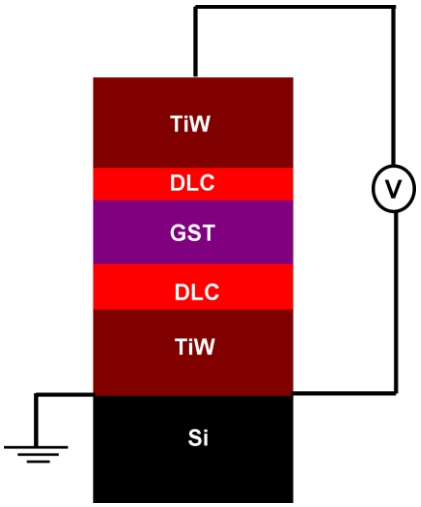

Fig. 1. The layered structure of the phase-change memristor

The memristive behaviour of the phase-change memristor results from a combination of the electrical process, thermal process, and phase-transformation process. Consequently, in order to accurately predict the physical performance of the phase-change memristor, a comprehensively computational model that can simulate all the physical processes occurring inside the GST region needs to be developed. Here the Laplace equation is introduced to be responsible for the electrical process, which is given below.

$$\nabla \cdot (\sigma \cdot \nabla V) = 0, \tag{1}$$

where σ is the electrical conductivity of the GST region, and V is the electric potential. It should be noted that there is a significant difference on the electrical conductivity between amorphous phase and crystalline phase. In this case, we assume that the electrical conductivity of the amorphous GST is governed by the Poole-Frenkel (PF) mechanism, thus giving [21]:

$$\sigma_{am} = \left(\frac{2k_B T}{q j_0 \Delta z} e^{\frac{E_A}{k_B T}} \operatorname{csc} h\left(\frac{qF\Delta z}{2k_B T}\right)\right)^{-1} \tag{2}$$

where F is the electric field, Δz is the average distance, E_A is the active energy for PF conduction, K_B is the Boltzmann constant, q is the electron charge, and T is the temperature. Differing from the amorphous GST, the crystalline GST usually exhibits an Arrhenius-type electrical conductivity, which is described as [22]:

$$\sigma_{cryst} = \sigma_{0_{cryst}} e^{\frac{-E_C}{k_B T}} \tag{3}$$

where σ_{0cryst} is a constant and E_c is the active energy for crystallization. Figure 2 shows the electrical conductivities of the GST media at different phases as a function of the electric field and temperature, respectively.

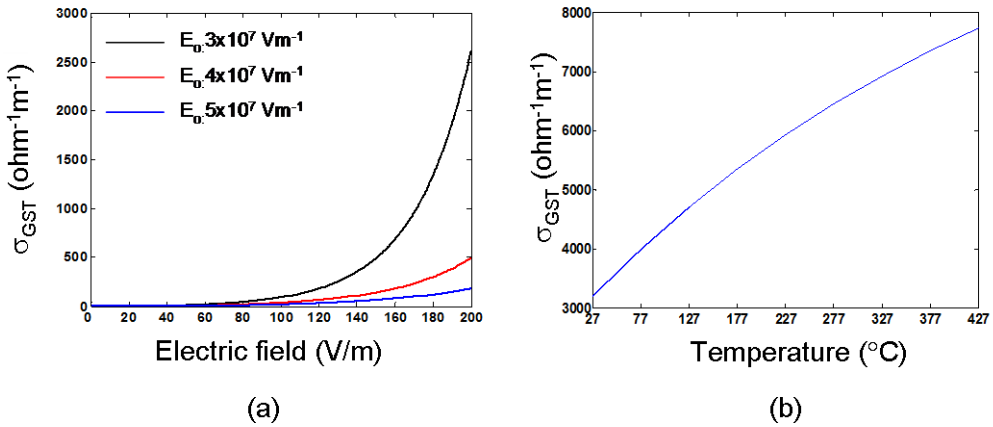

Figure 2. The electrical conductivity of (a) the amorphous GST as a function of the electric field at room temperature, and (b) the crystalline GST as a function of the temperature.

Solving the Laplace equation would result in a current distribution inside the GST media, which is the source of Joule heating for the thermal process. In this case, the classical heat transfer equation, as given in Eqn. (4), is adopted in this article to calculate the resulting temperature distribution inside the GST media.

$$\rho C_p \frac{\partial T}{\partial t} - K.\nabla^2 T = \sigma |F|^2 \tag{4}$$

where ρ, C_p, and K are the density, heat capacity, and thermal conductivity of the GST media respectively. Other parameters are as for Eqns (1)-(3). It should be noted that similar to electrical conductivities, the GST media exhibits a pronounced difference on the thermal conductivity between amorphous phase and crystalline phase. In order to take into account this effect, the thermal conductivity of the amorphous GST in our model is assumed to be a constant, while the thermal conductivity of the crystalline GST is considered to follow a power law to fit the experimental finding. The temperature dependent thermal conductivity of the crystalline GST is illustrated in Figure 3.

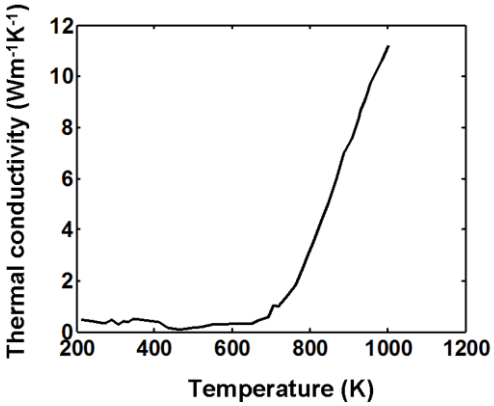

Fig. 3. Thermal conductivity of the crystalline GST as a function of temperature. Reprinted with permission from [21].

The resulting temperature distribution from the heat transfer equation is subsequently combined with the rate equation to describe the phase-transition process that takes place inside the GST media. Rate equation enables the calculation of the crystal fraction, given by:

$$\frac{df_x}{dt} = -(1 - f_x)k_x \tag{5}$$

where f_x is the crystal fraction and k_x is the thermal-activated kinetic constant, denoted as:

$$k_x = (t_{x1}e^{\frac{E_{x1}}{k_B T}} + t_{x2}e^{\frac{E_{x2}}{k_B T}})^{-1} \tag{6}$$

where t_{x1} and t_{x2} are pre-exponential factors, and E_{x1} and E_{x2} are temperature-dependent activation energies.

Based on the descriptions presented so far, the crystal fraction of the GST media can be obtained by simultaneously solving the Laplace equation, the heat transfer equation, and the rate equation. It should be however noted that as the GST media exhibits a phase-dependent electrical/thermal conductivity, they should vary along with the increase of the crystal fraction. Such a relationship in our model is described by:

$$\sigma_{GST} = \sigma_{am}(1 - f_x) + \sigma_{cryst} f_x \tag{7}$$

$$K_{GST} = K_{am}(1 - f_x) + K_{cryst} f_x \tag{8}$$

where σ_{GST} and K_{GST} are the electrical conductivity and thermal conductivity of the GST media. Circular symmetry is introduced into the developed model to reduce a full three-dimensional simulation to two dimensions, and all the calculations are performed using COMSOL MULTIPHYSICS™.

3. Results and discussions

A series of triangular up/down pulses are successively applied into the designed memristor device to investigate its memristive behaviour. Figure 4 shows the crystal fraction inside the GST media after each voltage pulse. As can be seen from Figure 4(a), crystallization phenomenon initiates from the interface between the DLC capping layer and the GST media after an application of a 3 V pulse of 100 ns. This is because the resulting temperature in this region is higher than elsewhere in the GST layer due to the low thermal conductivity of the DLC capping layer. As a result, more Joule heating is accumulated in this region, thus making the GST materials in this region readily achieve the crystallization temperature. Compared to the top interface, the bottom interface (i.e., interface between GST media and DLC bottom layer) exhibits a relatively low temperature. This is expected as the thermal conductivity of the bottom DLC is higher than that of the top DLC, thereby inducing a more severe heat dissipation effect. Such a difference on the temperature between the top interface and the bottom interface can be clearly noticed from Figure 5. After the application of the second excitation signal, the previously formed crystalline bit expands gradually to the surrounding region due to the growth of the

nucleis, which is depicted in Figure 4(b). However, owing to the fairly low temperature, the bottom region of the GST layer remains amorphous. Figure 4(c) and 4(d) show the crystal fraction of the GST layer after the third cycle and the fourth cycle, respectively. It is clearly indicated that along with the increase of the number of the cycles, the crystalline region has been experiencing a continuous growth from the top surface to the bottom surface, and the GST layer is fully crystallized after the fifth cycle, as illustrated in Figure 4(e).

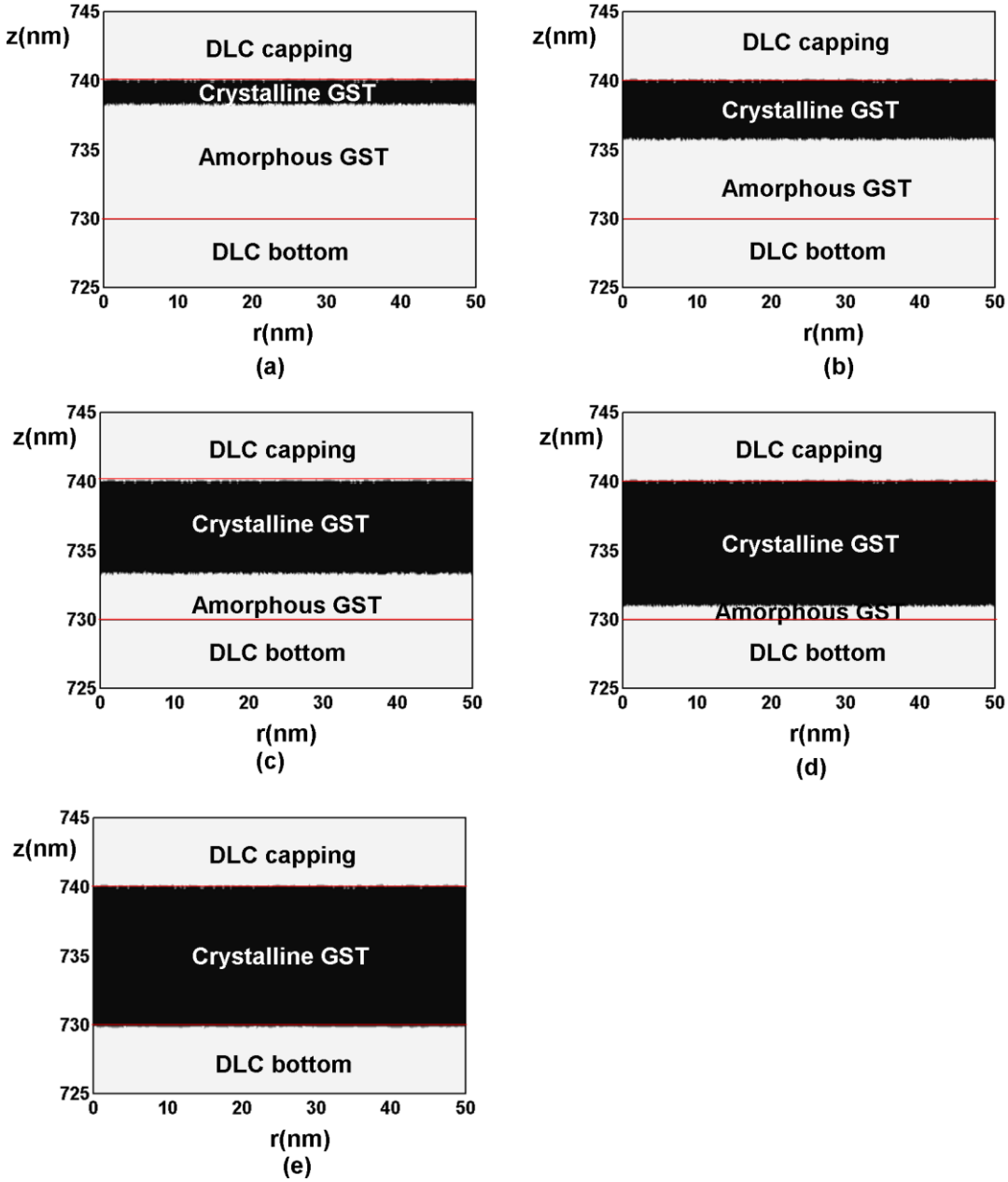

Fig. 4. The crystallization portion after (a) the first excitation cycle, (b) the second excitation cycle, (c) the third excitation cycle, (d) the fourth excitation cycle, and (e) the fifth excitation cycle.

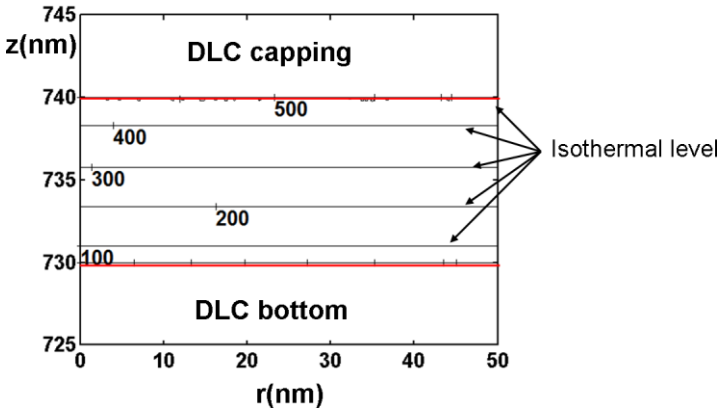

Fig. 5. Temperature profile (℃) inside the GST layer after the first excitation signal.

According to Figure 4, the resistance of the phase-change based memristor is changed due to the movement of the amorphous-crystalline boundary towards the amorphous region. This resembles the memristive mechanism of the TiO_2-based resistive memristor where the application of a voltage can cause the interface between doped and up-doped portions of active region to move back and forth. Therefore, the designed phase-change device undoubtedly enables an analogous memristive behaviour to the classical resistive memristor. In order to further verify this, we calculated the resulting I-V curve after each excitation pulse, which is illustrated in Figure 6. As can be seen from Figure 6, the calculated I-V curves from cycle 1 to cycle 4 exhibit a pinched hysteresis loop, while the last curve follows the linear Ohmic conduction. As the pinched hysteresis loop is considered as the most representative feature of the memristor device, results shown in Figure 6 have further demonstrated the capability of this phase-change based device to provide memristive function. After the last cycle, the GST layer has been fully crystallized, thus giving rise to a constant resistance. In this case, the consequent I-V curve shows a linear Ohmic behaviour. It is also informative in Figure 6 that the rising edge of the I-V curve of one excitation cycle does not exactly overlap the trailing edge of the preceding cycle, which is different from the conventional TiO_2 memristor. This can be ascribed to the different temperatures to be experienced by the chalcogenide layer during the rising and trailing curves of successive cycles. As the cooling rate of the GST for the rising edge of one cycle may differ from that of the trailing edge of the preceding cycle, the electrical conductivity of the GST that strongly replies on temperature may also vary between these two cases. This would result in different system resistance, thus separating one I-V curve from another. In spite of the different I-V curve from the classical conductive-front type of TiO_2 memristor, the proposed phase-change memristor allows for a similar memristive behaviour to the TiO_2 memristor that it remembers its present state and its previous state replies on the previous state. More importantly, compared to the classical resistive memristors, the memristor using chalcogenide alloy displays several merits. Firstly, the ability to provide long endurance cyclability up to 10^{12} using chalcogenide alloy has been demonstrated. In addition, the chalcogenide alloy provides an excellent retention time with 10 years at 85°C, while even longer lifetimes can be possibly accessed for constituent with higher crystallization temperature (e.g. GeTe, see Ref [23]). Moreover, the resistance state of the chalcogenide alloy can be toggled within nanosecond or even picosecond regime, giving rise to a fast switching speed. Finally, the feasibility of fabricating 3D cross-bar phase-change memory arrays has also been proven, opening a route for constructing massively parallel interconnected neuromorphic networks.

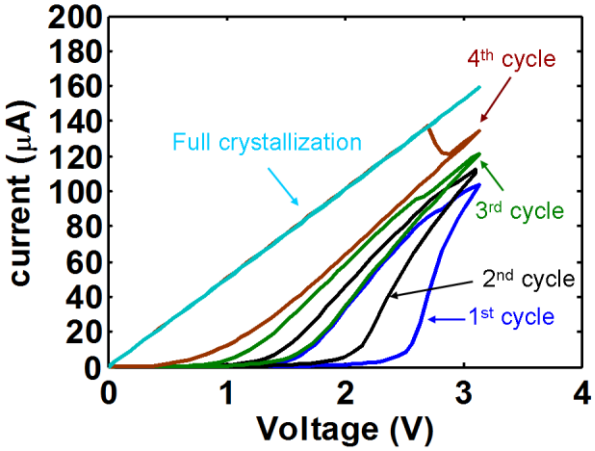

Fig. 6. I-V curves for each excitation cycle.

4. Conclusions

A pseudo-3D computation model has been developed to investigate the memristive function of the nanoscale phase-change device by simultaneously solving the Laplace equation, the heat transfer equation, and the rate equation. Results reveal that the crystal fraction of the GST layer gradually moves from the top DLC/GST interface towards the bottom DLC/GST interface, resembling the moving conductive-front phenomenon of the TiO_2 resistive memristor. The calculated I-V curves exhibit a pinched hysteresis loop, further demonstrating its ability to provide memristive function. The proposed phase-change device also allows for several advantages such as low power consumption, long data retention, and strong endurance cycle when compared to other memristor devices.

Acknowledgements

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