

## STRUCTURAL AND ELECTRICAL PROPERTIES OF $\text{Pb}_{1.1}(\text{Zr}_{0.20}\text{Ti}_{0.80})\text{O}_3$ FILMS ON Si WITH ZnO BUFFER LAYERS FOR FERROELECTRIC FETs APPLICATIONS

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Metal-Ferroelectric-Insulator-Semiconductor (MFIS) capacitors were fabricated using Au/ $\text{Pb}_{1.1}\text{Zr}_{0.20}\text{Ti}_{0.80}\text{O}_3$  / ZnO/ Si (100) structure. Zinc oxide (ZnO) thin film used as an insulating buffer layer deposited on n-type Si (100) substrate by thermal evaporation method. Lead zirconate titanate ( $\text{Pb}_{1.1}\text{Zr}_{0.20}\text{Ti}_{0.80}\text{O}_3$ ) films were prepared as a ferroelectric layers by sol- gel route. The surface features were revealed using Scanning Electron Microscope (SEM). The leakage current density of the ZnO/n-Si (100) structure was as low as  $1.8 \times 10^{-8}$  A/cm<sup>2</sup> at 2.5 V, which indicates excellent insulating property of the buffer layer. The capacitance - voltage (C-V) characteristics of the annealed ZnO/Si (MIS) structure indicated the good interface properties and the buffer layer with the substrate does not show hysteresis behavior. The stack layers PZT (140nm) and ZnO (60nm) thickness were appropriately optimized. Au/PZT/ZnO/Si Leakage-current density was about  $3.7 \times 10^{-5}$  A/cm<sup>2</sup> at positive bias voltage 3V. Good memory window width (2.2 V) was measured in C-V curve of Au/PZT/ZnO/Si capacitor with a voltage sweep of 12 V, after annealing at 700°C for 30 min in air atmosphere. Value of optical band gap (PZT) was found to be 3.46 eV. This experimental results show that the PZT-ZnO based MFIS structure is suitable for non-volatile ferroelectric memory field-effect-transistors (FETs) with large memory window.

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### 1. Introduction

FET (field effect transistor)-type ferroelectric random access memories (FeRAM) have recently attracted attention for non-destructive read-out (NDRO) type nonvolatile memory applications with low operation voltage [1-2]. Ferroelectric PZT films are a promising candidate for future FeRAM, which is non-volatile memory that uses ferroelectric material in order to maintain an electric charge [3]. This memory may be classified as two types. One is the capacitor type ferroelectric memory where the capacitor is the storage element and another is single transistor type ferroelectric memory where the storage element is the ferroelectric gate of the transistor. In order to realize ferroelectric FETs, preparation of ferroelectric/Si structures with a sharp interface is essential. However, it is very difficult to deposit the ferroelectric PZT films directly on silicon substrates without interfacial reaction, because Pb is highly reactive with Si and easily diffuses into the Si substrates [4]. An undesirable Si oxide is formed between the insulator and the Si substrate during high- temperature annealing for ferroelectric crystallization. The interfacial  $\text{SiO}_x$  brings an additional series capacitors problem, which reduces the total capacitance and the actual voltage applied to the ferroelectrics. In addition, a large electric field applied to interfacial  $\text{SiO}_x$  frequently causes significant charge injection and reliability problems [5, 6]. Therefore, it is an important to avoid formation of a  $\text{SiO}_x$  layer in order to reduce the series capacitance problem and to maintain high capacitance at the insulator layer. To solve these problems, a buffer layer is usually inserted between ferroelectric layer and silicon substrate,

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forming a metal-ferroelectric-insulator–semiconductor (MFIS) structure. Typical buffer-layer materials are  $\text{HfO}_2$  [7],  $\text{Y}_2\text{O}_3$  [8, 9],  $\text{CeO}_2$  [10],  $\text{Si}_3\text{N}_4$  [11],  $\text{Al}_2\text{O}_3$  [12],  $\text{TiO}_2$  [13] and  $\text{SrTiO}_3$  [14] which have relative high dielectric constants, low leakage current, good interface characteristics, and compatibility. Rajangam Ilangovan et al used  $\text{Al}_2\text{O}_3 - \text{HfO}_2$  buffer layer with SBT ferroelectric layer to improve the electrical properties [15, 16]. In the present work, a buffer layer of ZnO and PZT ferroelectric films were fabricated by thermal evaporation and sol-gel method, respectively. In order to show that the PZT-ZnO based MFIS structure is suitable for non-volatile memory FETs with large memory window, the electrical and structural properties of the MFIS structure at a relatively low processing temperature of  $700^\circ\text{C}$  were investigated.

## 2. Experimental work

N-type Si (100) wafers were used as substrates. After degreasing, the substrate was dipped into a solution of  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$  (= 4:1) to remove organic impurities then soaked in a hot solution of  $(\text{NH}_3 + \text{H}_2\text{O}):\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (= 0.05:1:5) to remove heavy metals. Subsequently, the substrate was dipped in diluted HF solution to remove  $\text{SiO}_2$  on the Si substrate. Then, ZnO films were deposited on n-type Si-substrates by thermal evaporation of pure ZnO powder (purity > 99.999%, Produced by Merck Ltd.). The ZnO pellet was placed on a tungsten basket in the evaporation system (HIND HI VAC Model No. 12 A4D Vacuum Coating Unit) and maintained approximately  $10^{-5}$  torr chamber pressure. During evaporation, the substrates were kept 15 mm above the source material. The as-deposited ZnO films were annealed in air using conventional tubular furnace at  $700^\circ\text{C}$  for 30 min. The  $\text{Pb}_{1.1}\text{Zr}_{0.20}\text{Ti}_{0.80}\text{O}_3$  films were deposited on ZnO/n-type Si (100) substrates by sol-gel route. The starting materials were Lead acetate trihydrate ( $\text{Pb}(\text{CH}_3\text{COO})_2 \cdot 3\text{H}_2\text{O}$ , 99.5% Loba chemicals), Titanium (IV) isopropoxide ( $\text{Ti}(\text{O}^i\text{Pr})_4$ , 99% Merck), and Zirconium acetylacetonate ( $\text{ZrC}_{20}\text{H}_{28}\text{O}_8$  99.8% Merck). 2-Methoxyethanol and acetic acid were used as a solvent and chemical modifier respectively. The molar ratio of Zr/Ti was 20/80. The concentration of PZT precursor solution is 0.4 M. Excess of Lead acetate (10%) was added to the solution to compensate the loss of lead during the thermal treatment. PZT thin films were prepared by spin coating with the speed of 3000 rpm for 20 seconds. After depositing by spin coating, the gel films were pyrolyzed in air at  $300^\circ\text{C}$  for 10 min to remove solvent and other organics. These processes were repeated for several times for getting desired film thickness. Finally, the PZT thin film was postannealed at  $600^\circ\text{C}$  and  $700^\circ\text{C}$  for 30 min in air. The thickness of the PZT films was 140 nm. For measurements of electrical properties, gold was used as a top electrode on  $\text{Pb}_{1.1}\text{Zr}_{0.20}\text{Ti}_{0.80}\text{O}_3/\text{ZnO}/\text{Si}$  structures by a vacuum evaporation method at room temperature through a shadow mask and the area was  $0.2\text{mm}^2$ . Silver paste was used as a bottom electrode of PZT/ZnO/Si structures.

Powder X-Ray Diffraction (XRD) analysis was carried out with Cu-K $\alpha$  radiation (Model XPERT-PRO). Microstructure and morphology of the thin films were observed using Scanning Electronic Microscope (SEM, Hitachi Model S-3000H). Capacitance – Voltage study was carried out by impedance analyzer (HP4194A) at 1 MHz with a small signal voltage of 100 mV. Leakage current density (J–V) measurements were done by Keithley 6517 electrometer. The optical study was performed by UV-VIS-NIR spectrophotometer (CARY 500 Scan Varian).

## 3. Results and discussions

Fig 1 shows the XRD patterns of the ZnO and Ti-rich  $\text{Pb}_{1.1}\text{Zr}_{0.20}\text{Ti}_{0.80}\text{O}_3/\text{ZnO}$  thin films on n-type Si substrate. The ZnO has the hexagonal structure as shown in figure 1, the ZnO thin film is found to have a well-formed structure of hexagonal and preferred orientation of (0002) direction in the out of plane direction after annealing at  $700^\circ\text{C}$  for 30 min. The crystalline quantity of ZnO thin films can be evaluated by the full width half maximum (FWHM) of (0002) peak at  $2\theta=34.65$ . The sol-gel derived Ti-rich PZT thin films were annealed at  $700^\circ\text{C}$  for 30 min. All PZT films on the ZnO/Si film exhibited polycrystalline growth. Additionally, these films showed more significant (100) orientation especially when the Ti content increased from 0.48 to 0.80. No undesirable peak of pyrochlore phase appeared in the XRD patterns, which shows that PZT films are well crystallized with perovskite structure with preferred orientation of (111) peak at  $2\theta=38.26$ .

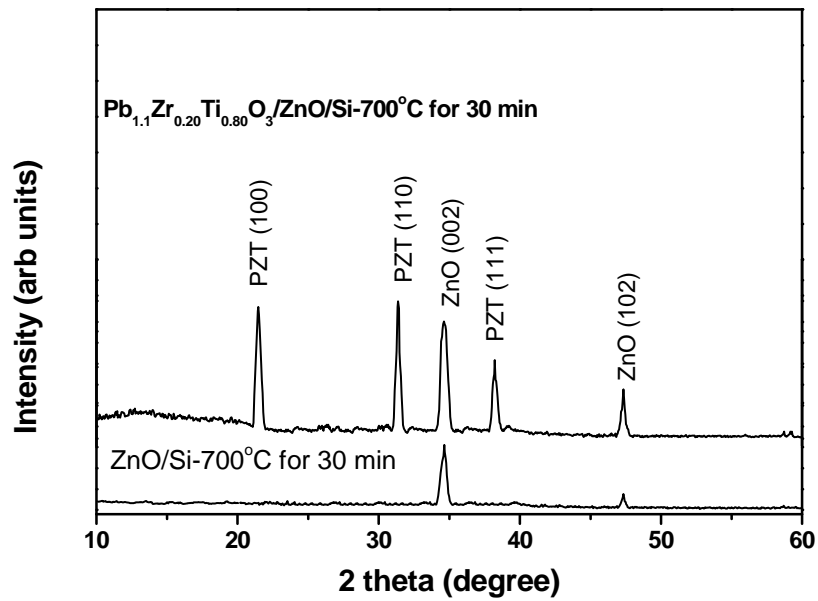


Fig. 1. XRD patterns of the  $Pb_{1.1}Zr_{0.20}Ti_{0.80}O_3/ZnO/n-Si$  and  $ZnO/n-Si$  thin films.

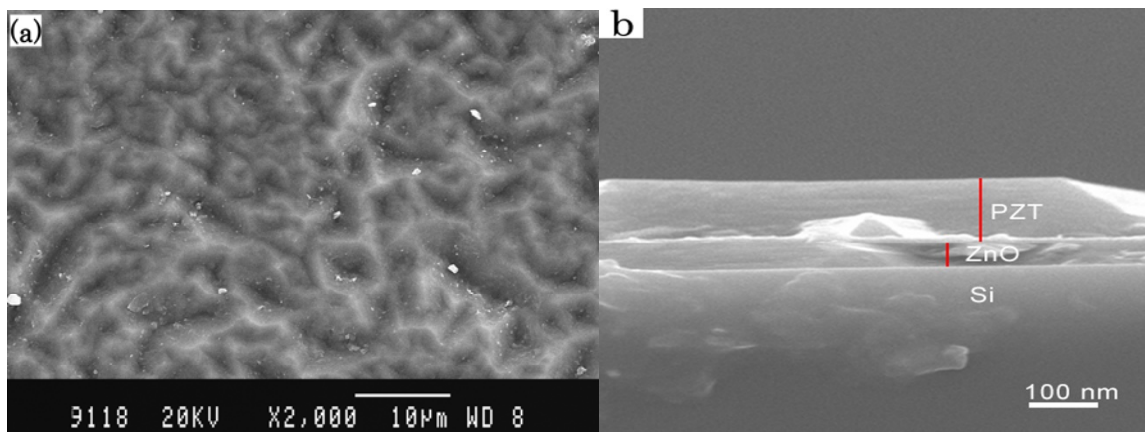


Fig. 2. SEM images of the a) surface b) cross -section view of  $PZT/ZnO/Si$  thin films.

Figure 2 shows SEM images of surface and cross-section view of the  $Pb_{1.1}Zr_{0.20}Ti_{0.80}O_3/ZnO/Si$  thin films annealed at  $700^\circ C$  for 30 mins. Figure 2 a) shows that the films have the dense, crack-free and an island like hazy surface. The smooth and dense surface is also an evidence for the complete formation of perovskite structure. Thickness of the PZT film (140nm) and ZnO film (60 nm) were estimated from the SEM image (figure 2 b).

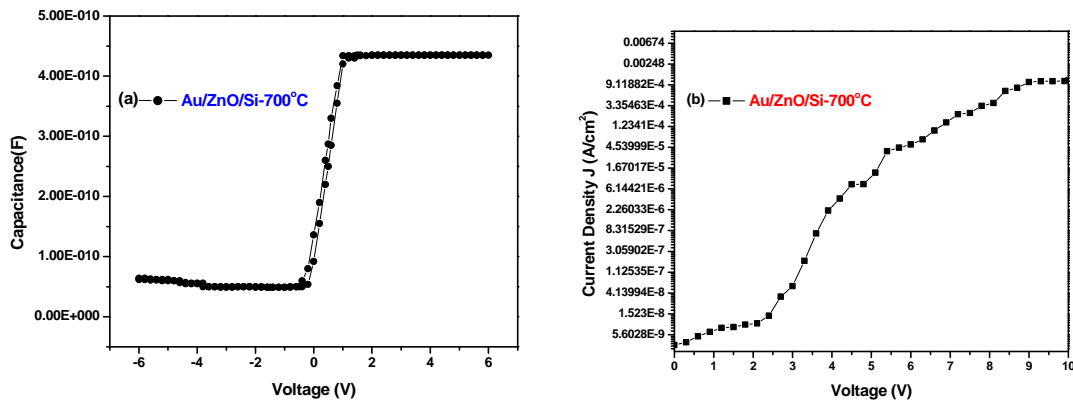


Fig. 3. C-V (a) and J-V (b) characteristics of Au/ZnO/Si (100) (MIS) diodes at annealed at 700°C for 30 min.

Figure 3(a) shows a typical Capacitance-Voltage (C-V) characteristics at room temperature for an Au/ZnO/Si capacitor measured at 1MHz with a small signal voltage of 100mV and the sweep rate of 0.2V/s for all the bias voltage. The C-V curve clearly shows the region of accumulation, depletion and inversion. The accumulation region capacitance is read to be approximately 430pF. The width of the loop was 0.2V, which shows that ZnO layer served as a good buffer layer and there is no threshold hysteresis which was apparent in the C-V curve. Figure 3(b) shows J-V characteristics of Au/ZnO/Si structure as a function of deposition temperature, which was measured with a sweep rate of 0.3 V and delay time of 0.8 sec. The current density at 2.5 V is about  $1.8 \times 10^{-8}$  A/cm<sup>2</sup>, which indicates that the process technique resulted good buffer layer with highly insulating property of the deposited ZnO film layer of MFIS structure which is relatively good for memory device applications.

Figure 4 shows J-V characteristics of Au/ Pb<sub>1.1</sub>Zr<sub>0.20</sub>Ti<sub>0.80</sub>O<sub>3</sub>/ZnO/n-Si (MFIS) structure annealed at 700°C for 30 mins, which was measured with a voltage step of 0.3 V and delay time of 0.8 sec. Figure 4 shows that the leakage-current density is about  $3.7 \times 10^{-5}$  A/cm<sup>2</sup> at positive bias voltage 3 V.

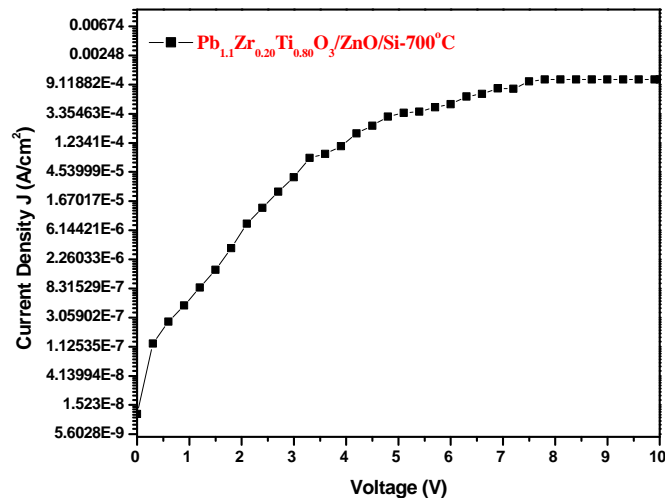


Fig. 4. Leakage current density (J-V) characteristic of Au/PZT/ZnO/n-Si capacitor structure.

It causes due to higher temperature treatment PZT film diffuse or overlying ZnO buffer of lead during higher thermal treatment. The experimental results show that the PZT/ZnO based bias voltage 3 V. It causes due to higher temperature treatment PZT film diffuse or overlying ZnO buffer layer. On the other hand, this might be on account of lead deficiency that means loss of lead during higher thermal treatment. The experimental results show that the PZT/ZnO based MFIS structures are suitable for non-volatile FET- type ferroelectric memory application especially for low voltage (<3V), low power dissipation operation in the devices.

Figure 5 (a) shows a typical curve of the 1 MHz  $C-V$  characteristic for the Au/Pb<sub>1.1</sub>Zr<sub>0.20</sub>Ti<sub>0.80</sub>O<sub>3</sub>/ZnO/ Si (100) structure annealed at 700°C for 30 mins. The maximum memory window were measured at different bias voltages, with sweep rate at the bias voltage was 0.2V/s. The counterclockwise  $C-V$  hysteresis loop indicated by arrows in the figure is observed. This suggests that the hysteresis resulted from the switching of the ferroelectric polarization of PZT films, rather than charge trapping. Theoretically, the memory window of the ferroelectric gate structure should be equal to twice of the coercive voltage, but the memory

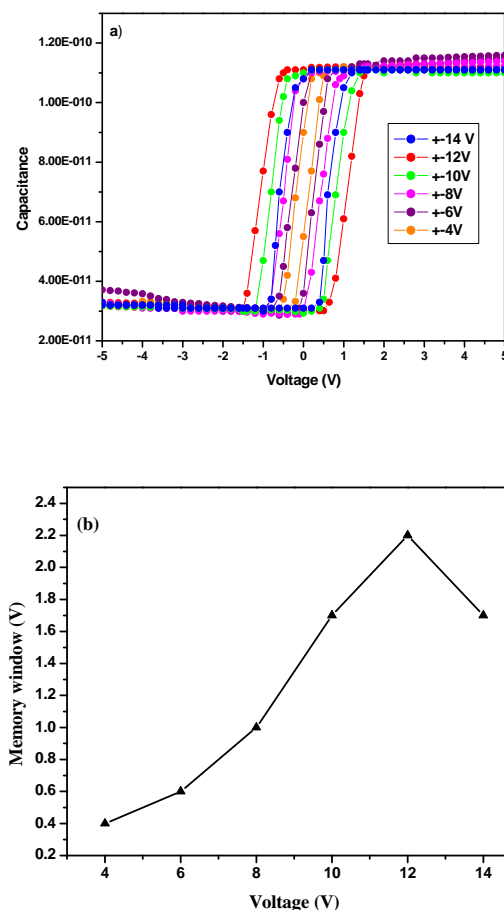


Fig. 5. (a) Capacitance-Voltage curve b) Memory window of the Au/PZT/ZnO/Si (MFIS) structure annealed at 700°C for 30 min.

window is related to the mobile ions, coercive field, saturation level of the polarization, rearrangement of the space charge and interfacial polarization [9, 17], and is also affected by the crystal orientation, film thickness and grain size of the ferroelectric thin film. In our  $C-V$  experimental results, the counterclockwise hysteresis loops are observed and width of the loop increases as the gate voltage increases [18-20]. The width of the loops of Au/PZT/ZnO/n-Si (100) capacitor increased from 0.4 to 2.2 V with increasing the applied voltage from 4 to 12 V. Further

increasing the bias voltage up to  $\pm 14$  V the memory window decreased (figure 5b & c). This is due to the charge injection into the ZnO because much higher electric field is applied to the ZnO layer. This memory window satisfies (2.2V) the practical application of FET type non-destructive read out (NDRO) ferroelectric random access memories (FeRAMs) operation.

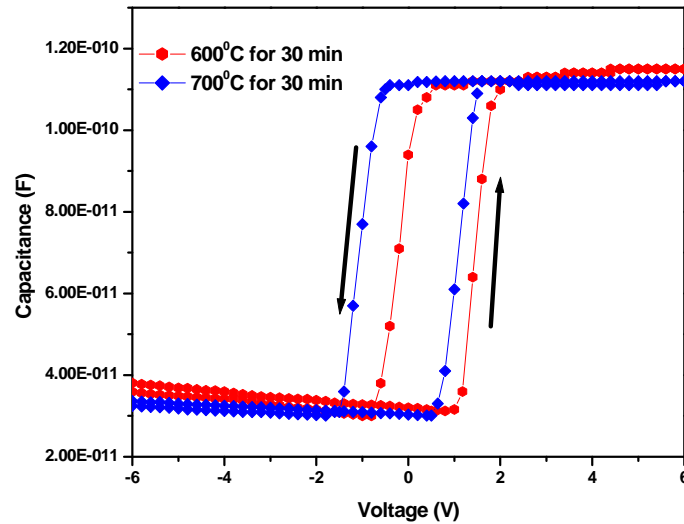


Fig. 6. C-V curve for Au/  $Pb_{1.1}Zr_{0.20}Ti_{0.80}O_3/ZnO/Si$  at  $600^\circ C$  and  $700^\circ C$  for 30 min.

Figure 6 shows the C-V characteristics curve of Au/PZT/ZnO/n- Si (100) capacitor at various annealing process. At  $700^\circ C$ , the memory window was 2.2 V, further increasing the temperature to  $750^\circ C$  the memory window width decreased to 1.6 V, which depicts that there may be a lead deficiency in the ferroelectric structure, which means loss of lead during higher thermal treatment. In addition, we have studied the optical properties of PZT thin film. The PZT thin film was directly deposited on corning glass by sol-gel route and annealed at  $600^\circ C$  for 30 mins. A graph between  $(\alpha hv)^2$  vs.  $hv$  was plotted as shown in Figure 7 and the band gap of the PZT film was found to be 3.46 eV ( $\alpha$  absorption coefficient,  $hv$  incident photon energy). This is in good agreement with a band gap of 3.4 eV reported by S.K. Pandey et al [21].

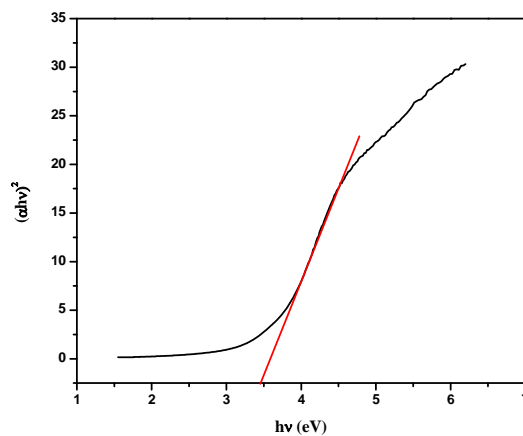


Fig. 7.  $(\alpha hv)^2$  vs.  $hv$  plot showing optical band gap.

#### 4. Conclusion

PZT films have been grown on Si substrates with ZnO buffer layers using sol-gel route. The capacitance–voltage (C-V) curve of Au/ZnO/Si (MIS) clearly shows the region of accumulation, depletion and inversion and there is no threshold hysteresis observed and the leakage current is  $1.8 \times 10^{-8}$  A/cm<sup>2</sup>, it indicates that ZnO buffer layer serves as a good insulating property for the fabrication of PZT/ZnO/Si memory devices. Au/PZT/ZnO/Si (MFIS) leakage-current density was about  $3.7 \times 10^{-5}$  A/cm<sup>2</sup> at positive bias voltage 3V. In the capacitance–voltage (C-V) characteristics of Au/Pb<sub>1.1</sub>Zr<sub>0.20</sub>Ti<sub>0.80</sub>O<sub>3</sub>/ZnO/n-Si (100) structures, a hysteresis loop with counterclockwise trace was observed and the memory window was about 2.2 V. The optical band gap of PZT was 3.46 eV. Therefore, it can be concluded that the Au/PZT/ZnO/Si structure prepared in this work is promising for ferroelectric FETs applications.

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